

**REMARKS**

Claims 1-22 and 33-60 are currently pending. Claims 1, 4, 9, 15-16, 33, 41, 47-48 and 55 are amended, without acquiescence or prejudice to pursue the original claims in a related application. Claims 3 and 35 are cancelled, without acquiescence or prejudice to pursue the original claims in a related application. No new matter has been added.

**Claim Rejections Under 35 U.S.C. §101**

Claims 1-22 and 33-60 were rejected under 35 U.S.C. §101 for being directed to non-statutory subject matter. In response, these claims have been amended to address the rejection, without acquiescence or prejudice to pursue the original claims in a related application. Thus, Applicants respectfully request reconsideration of these claims and withdrawal of the rejections.

**Claim Rejections-35 U.S.C. §103**

Claims 1-13, 15-19, 21-22, 33-45, 47-51, 53-55, 57-58 and 60 were rejected under 35 U.S.C. §103(a) as unpatentable over Passerone (“Fast Hardware/Software Co-Simulation for Virtual Prototyping and Trade-Off Analysis”, 1997, Proceedings of Design Automation Conference 1997) in view of Hellestrand (U.S. Patent No. 6,230,114).

Claims 14 and 46 were rejected under 35 U.S.C. §103(a) as unpatentable over Passerone in view of Hellestrand and Hartoog (“Generation of Software Tools from Processor Descriptions for Hardware/Software Codesign”, Proceedings of the 34<sup>th</sup> Design Automation Conference, June 9-13, 1997).

Claims 20, 52 and 59 were rejected under 35 U.S.C. §103(a) as unpatentable over Passerone in view of Hellestrand and Suzuki (“Efficient Software Performance Estimation Methods for Hardware/Software Codesign”, 1996, Proceedings of the 33<sup>rd</sup> Annual Conference on Design Automation).

In response, Applicants respectfully traverse.

Independent claim 1 recites the following limitations (emphasis added):  
describing a system design as a network of logical entities;

selecting at least one of the logical entities for a software implementation;  
implementing a source software program for the logical entities selected for the software implementation;  
compiling the software program to generate an optimized assembler code representation of the software program;  
performing a performance analysis using the assembler code;  
*generating an assembler-level C software simulation model using the assembler code;*  
generating a hardware/software co-simulation model using the software simulation model; and  
storing at least the hardware/software co-simulation model.

Applicants respectfully submit that the cited references do not disclose each and every limitation of present independent claim 1.

In section 11.3.2, the Action concedes that Passerone does not disclose or suggest, “generating a software simulation model using the assembler code”, in a manner as recited in independent claim 1, prior to the amendments presented herein. In section 11.10, the Action purports that Passerone appears to teach that, “the software simulation model is an assembler-level C code simulation model”, in a manner as recited in claim 3, prior to the amendments presented herein. However, due to the dependency of the subject matter of claim 3 on the subject matter of claim 1, Applicants assert that Passerone fails to teach that, “the software simulation model is an assembler-level C code simulation model.”

In section 11.4.2, the Action purports that Hellestrand, in col. 32, lines 14-36, appears to teach, “generating a software simulation model using the assembler code”, in a manner as recited in independent claim 1, prior to the amendments presented herein.

However, Applicants respectfully disagree. Applicants assert that Hellestrand fails to disclose, “generating an assembler-level C code software simulation model using the assembler code”, as recited in present independent claim 1.

In the passage referenced by the Action in section 11.4.2, Hellestrand discloses, in col. 32, lines 14-36, re-parsing the original user C program file by inserting a set of static

arrays to include the timing and size of each block, statements in each block to increment a global delay counter for that block, calls for timing that is not determined until runtime, and statements to maintain line numbering. The results of this second merge is an analyzed user C program file. Clearly, Hellestrand generates an analyzed user C program file using the original user C program file and merely back-annotates source code with timing information. Accordingly, Hellestrand does not disclose generating an assembler-level C code software simulation model using the assembler code, as recited in present independent claim 1.

In contrast to Hellestrand, present independent claim 1 recites, “compiling the software program to generate an optimized assembler code representation of the software program; performing a performance analysis using the assembler code; ***generating an assembler-level C software simulation model using the assembler code;*** generating a hardware/software co-simulation model using the software simulation model; and storing at least the hardware/software co-simulation model. Hellestrand does not disclose these features in a manner as claimed by the Applicants in present independent claim 1.

For at least these reasons, it is respectfully submitted that independent claim 1 is patentable over the cited references.

For at least these same reasons, it is respectfully submitted that independent claims 9, 33, 41 and 55 are likewise patentable over the cited references.

The remaining claims are considered patentable over the cited references for at least their respective dependence on independent claims 1, 9, 33, 41 and 55.

**CONCLUSION**

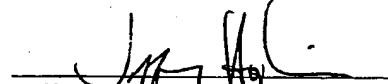
Based on the foregoing, all claims are believed allowable, and an allowance of the claims is respectfully requested. If the Examiner has any questions or comments, the Examiner is respectfully requested to contact the undersigned at the number listed below.

The Commissioner is authorized to charge any fees due in connection with the filing of this document to Bingham McCutchen's Deposit Account No. 50-2518, referencing billing number 7012162001. The Commissioner is authorized to credit any overpayment or to charge any underpayment to Bingham McCutchen's Deposit Account No. 50-2518, referencing billing number 7012162001.

Respectfully submitted,  
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